Solution Manual for CMOS Digital Integrated Circuits Analysis and Design 4th Edition Kang Leblebici Kim

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Exercise Problems

3.1 Consider a MOS system with the following parameters:

$$t_{ox} \quad 1.6\text{nm}$$
$$_{GC} \quad 1.04\text{V}$$
$$N_A = 2.8\ 10^{18}\ \text{cm}^{-3}$$
$$Q_{OX} \quad q\ 4\ 10^{10}\ \text{C/cm}^2$$

a. Determine the threshold voltage V_{T0} under zero bias at room temperature (T = 300 K).

Note that $_{ox}$ 3.97 $_0$ and $_{si}$ 11.7 $_0$.

SOLUTION :

First, calculate the Fermi potentials for the p-type substrate and for the n-type polysilicon gate:

$$_F(substrate) \quad \ln \frac{kT}{q} \frac{n_i}{N_A} \quad 0.026\text{V} \ln \frac{1.45\ 10^{10}}{2.8\ 10^{18}} \quad 0.49\text{V}$$

The depletion region charge density at $V_{SB} = 0$ is found as follows:

$$Q_{B0} \quad \sqrt{2\ q\ N_A \quad Si \mid 2\ _F(substrate) \mid}$$
$$\sqrt{2\ 1.6\ 10^{19}\ (2.8\ 10^{18})\ 11.7\ 8.85\ 10^{14}\ 2\ 0.49\ 9.53 \mid}$$
$$10^{7}\ \text{C/cm}^2$$

The oxide-interface charge is:

$$Q_{ox} \quad q\ N_{ox} \quad 1.6\ 10^{19}\ \text{C} \quad 4\ 10^{10}\ \text{cm}^{-2} \quad 6.4\ 10^{9}\ \text{C/cm}^2$$

The gate oxide capacitance per unit area is calculated using the dielectric constant of silicon dioxide and the oxide thickness t_{ox}.

$$C_{ox} \quad \frac{_{ox}}{t_{ox}} \quad \frac{3.97\ 8.85\ 10^{14}\ \text{F/cm}}{1.6\ 10^{7}\ \text{cm}} \quad 2.2 \quad 10^{6}\ \text{F/cm}^2$$

Now, we can combine all components and calculate the threshold voltage.

$$V_{T0} \quad _{GC} \quad 2_{F}(substrate) \quad \frac{Q_{B0}}{C_{ox}} \quad \frac{Q_{ox}}{C_{ox}}$$

$$1.04 \quad (0.98) \quad (0.53) \quad (0.03) \quad 0.44V$$

b. Determine the type (p-type or n-type) and amount of channel implant (N_I/cm^2) required to change the threshold voltage to 0.6V

SOLUTION :

p-type implanted needed in the amount of:

$$V \quad 0.6 \quad V_{T0} \quad 0.6 \quad 0.44 \quad 1.04 \quad \frac{qN_I}{C_{ox}}$$

$$1.04\,C \qquad \frac{1.04\,2.2\ 10^{-6}}{}$$

$$N_I \quad \frac{C_{ox}}{q} \qquad 1.43\ 10^{13}\ \text{cm}^{-2}$$

3.2 Consider a diffusion area that has the dimensions $0.4 \quad m \quad 0.2 \quad m$ and the abrupt junction depth is $32\ nm$. Its n-type impurity doping level is $N_D = 2\ 10^{20}\ cm^{-3}$ and the surrounding p-type substrate doping level is $N_A = 2\ 10^{20}\ cm^{-3}$. Determine the capacitance when the diffusion area is biased at 1.2V and substrate is biased at 0V. In this problem, assume that there is no channel-stop implant.

SOLUTION :

$$C_j(V) \quad A \sqrt{\frac{_{si}\ q}{2} \quad \frac{N_A\ N_D}{N_A \quad N_D \quad _0\ V}} \quad \frac{1}{\sqrt{\quad}}$$

$$_0 \quad \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \quad 0.026 \ln \frac{2\ 10^{20}\ 2\ 10^{20}}{(1.45\ 10^{10})^2} \quad 1.21$$

$$A \quad 0.2 \quad 0.4 \quad 2\ 0.2 \quad 0.032 \quad 2\ 0.4 \quad 0.032 \quad 1.18\ 10^{-9}\ [\,cm^2\,]$$

$$C_j(V) \quad 1.18\ 10^{-9} \sqrt{\frac{11.7\ 8.854\ 10^{-14}\ 1.6\ 10^{-19}\ 4\ 10^{40}}{2 \qquad\qquad 4\ 10^{20}}} \quad \frac{1}{\sqrt{1.21 \quad 1.2}}$$

$$2.18\ 10^{-15}[F]$$

3.3 Describe the relationship between the mask channel length, L_M, and the electrical channel length, L. Are they identical? If not, how would you express L in terms of L_M and other parameters?

SOLUTION :

The electrical channel length is related to the mask channel length by:

$$L \quad L_M \quad 2L_D$$

Where L_D is the lateral diffusion length.

3.4 How is the device junction temperature affected by the power dissipation of the chip and its package? Can you describe the relationship between the device junction temperature, ambient temperature, chip power dissipation and the packaging quality?

SOLUTION :

The device junction temperature at operating condition is given as $T_j \; T_a \; P_{diss}$, where T_a is the ambient temperature; P_{diss} is the power dissipated in the chip; is the thermal resistance of the packaging.
A cheap package will have high which will result in large and possibly damaging junction temperature. Thus the choice of packaging must be such that it is both economic and pretective of the device.

3.5 Describe the three components of the load capacitance C_{load} , where a logic gate is driving other fanout gates.

SOLUTION :

The three major components of the load capacitance are interconnect capacitance, the next stage input capacitance, i.e., the gate capacitance and the drain parasitic capacitances of the current stage.

3.6 Consider a layout of an nMOS transistor shown in Fig. P3.6.
The process parameters are:

$N_D \quad 2\ 10^{20}\ \text{cm}^{3}$

$N_A \quad 2\ 10^{20}\ \text{cm}^{3}$

$X_j \quad 32\text{nm}$

$L_D \quad 10\text{nm}$

$t_{ox} \quad 1.6\text{nm}$

$V_{T\,0} \quad 0.53\text{V}$

Channel stop doping 16.0 (*p type substrate doping*)

Find the effective drain parasitic capacitance when the drain node voltage changes from 1.2V to 0.6V.

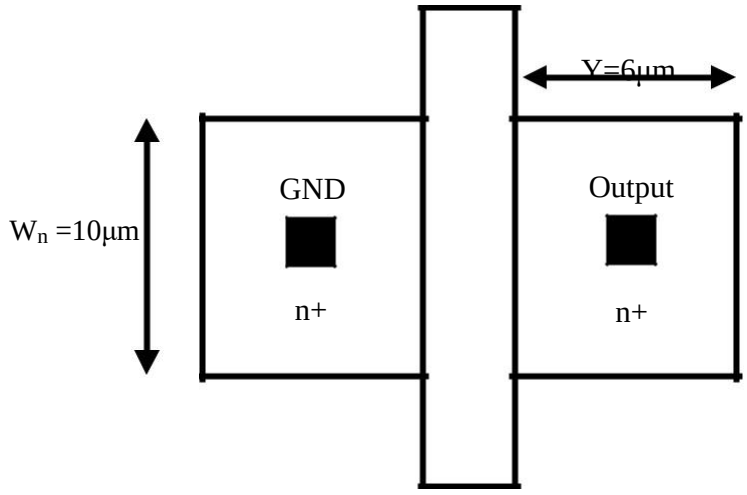


Figure P3.6

SOLUTION :

$$_0 \quad \frac{kT}{} \ln \frac{N_A N_D}{2} \quad 0.026 \ln \frac{2\ 10^{20}\ 2\ 10^{20}}{10^{\ 2}} \quad 1.21$$

$$q \quad n_i \quad (1.45\ 10\ )$$

$$_{osw} \quad \frac{kT}{} \ln \frac{N \cdot N}{2} \quad 0.026 \ln \frac{16\ 2\ 10^{20} \quad 2 10^{20}}{10^{\ 2}} \quad 2.31$$

$$q \quad n_i \quad (1.45\ 10\ )$$

$$C_{j\,0} \sqrt{\frac{_{si}\ q}{2} \frac{N_A\ N_D}{N\ N_A\ N_D}} \frac{1}{\sqrt{\ }} \quad _0$$

$$\sqrt{\frac{11.7\ 8.854\ 10^{\ 14}\ 1.6\ 10^{\ 19}\ 10^{20}}{1.21}} 2.61\ 10^{\ 6}\ [\mathrm{F/cm}^{\ 2}]^{\ 2}$$

$$C_{josw} \sqrt{\frac{_{si}\ q}{2} \frac{N_A' N_D}{N_A \quad N_D}} \frac{1}{\sqrt{\ }} \quad _{osw}$$

$$\sqrt{\frac{11.7\ 8.854\ 10^{\ 14}}{2.31}} \frac{1.6\ 10^{\ 19}}{} \frac{1.88\ 10^{20}}{} 2.59\ 10^{\ 6}\ [\mathrm{F/cm}^{\ 2}]^{\ 2}$$

$$C_{jsw} \quad X_j \, C_{josw} \; 32 \;\; 10^{9} \quad 2.59 \;\; 10^{6} \quad 0.083[\text{pF/cm}]$$

$$A \; Y \;\; W \;\; 6 \;\; 10 \;\; 60[\;\; m^2\,]$$

$$P \;\; 2(Y \;\; W) \;\; 2(6 \;\; 10) \;\; 32[\;\; m]$$

$$K_{eq} \quad 2\sqrt{\;_0} \; \frac{\sqrt{\;_0 \; 5} \quad \sqrt{\;_0 \quad 2.5}}{5 \;\; 2.5}$$

$$2\sqrt{0.8967} \quad \frac{\sqrt{5.8967} \;\; \sqrt{3.3967}}{2.5} \quad 0.44$$

$$K_{eq}' \quad 2\sqrt{\;_0} \; \frac{\sqrt{\;_0 \; 5} \quad \sqrt{\;_0 \quad 2.5}}{5 \;\; 2.5}$$

$$2\sqrt{0.8967} \quad \frac{\sqrt{5.8967} \;\; \sqrt{3.3967}}{2.5} \quad 0.44$$

$$C_{drain} \;\; Keq \; Cj\,0 \; A \quad Keq' \; Cjsw \; P$$

$$0.44 \; 9.6 \; 10^{9} \; 60 \; 10^{8} \; 0.46 \; 1.847 \; 10^{12} \; 32 \; 10^{4} \; 5.25[\; fF\;]$$

3.7 A set of *I-V* characteristics for an nMOS transistor at room temperature is shown for different biasing conditions. Figure P3.7 shows the measurement setup.
Using the data, find : (a) the threshold voltage V_{T0} and, (b) velocity saturation v_{sat}.

Some of the parameters are given as: W=0.6 m, E_cL=0.4 V, , t_{ox} = 16 Å, |2 $_F$| = 1.1 V.

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D(A)
0.6	0.6	0.0	6
0.65	0.6	0.0	12
0.9	1.2	0.3	44
1.2	1.2	0.3	156

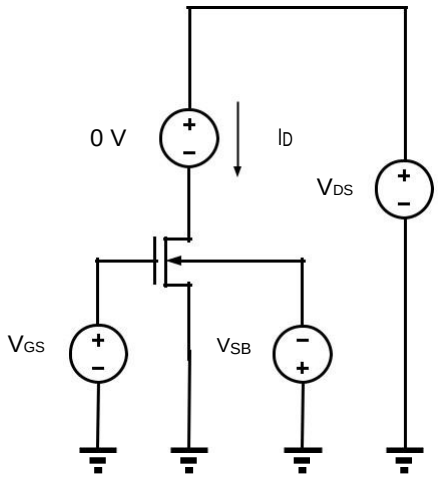


Figure P3.7

SOLUTION :

(a)

First, the MOS transistor is on ($I_D > 0$) for $V_{GS} > 0$ and $V_{DS} > 0$. Thus, the transistor must be an n-channel MOSFET. Assume that the transistor is enhancement-type and, therefore, operating mode.

$$I_D = W v_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{V_{GS} - V_T + V_c}$$

When V_{GS} and V_T are similar, velocity saturation terms are neglected.

Let (V_{GS1}, I_{D1}) and (V_{GS2}, I_{D2}) be any two current-voltage pairs obtained from the table. Then, the V_{T0}, can be calculated.

$$\frac{I_{D1}}{I_{D2}} = \frac{(V_{GS1} - V_{T0})^2}{(V_{GS2} - V_{T0})^2} \quad V_{T0} = \frac{\sqrt{\frac{6\ A}{12\ A}}\,0.65V - 0.6V}{\sqrt{\frac{6\ A}{12\ A}} - 1} = 0.48V$$

(b)

Find velocity saturation

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \cdot 8.85 \cdot 10^{-14}}{0.16 \cdot 10^{-8}} = 216 \cdot 10^{-4}\ F/m$$

$$I_D = \frac{(V_{GS} - V_T)^2}{V_{GS} - V_T + V_c}$$

$$12 \cdot 0.6 \cdot 10^{-6} = v_{sat} \cdot 216 \cdot 10^{-6} \cdot \frac{0.17^2}{0.17 + 0.4(1 + 0.05 \cdot 0.6)}$$

$$v_{sat} = 1.06 \cdot 10^{6}\ m/s$$

3.8 Compare the two technology scaling methods, namely, (1) the constant electric field scaling and (2) the constant power supply voltage scaling. In particular, show analytically by using equations how the delay

time, power dissipation, and power density are affected in terms of the scaling factor, S. To be more specific, what would happen if the design rules change from, say, 1 μm to 1/S μm (S>1)?

SOLUTION :

	Const . E field	*Const . V_{DD}*
W, L, t_{ox}	$1/S$	$1/S$
$\frac{V_{DD}}{}$	$1/S$	1
$\frac{}{C_{ox}}$	S	S
$C \quad C_{ox}WL$	$1/S$	$1/S$
k_n, k_p	S	S
$\frac{I_{DD}}{}$	$1/S$	S
$t_{delay} \quad \frac{C V}{I_{DD}}$	$1/S$	$1/S^2$
$Power \quad I_{DD}V_{DD}$	$1/S^2$	S
Power density $\frac{Power}{Area}$	1	S^3

3.9 A pMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D \; 1\;10^{16}\;\text{cm}^{-3}$, gate doping density (n-type poly) of $N_D \; 10^{20}\;\text{cm}^{-3}$, $Q_{ox} / q \; 4\;10^{10}\;\text{cm}^{-2}$, and gate oxide thickness of $t_{ox} \quad 1.6nm$. Calculate the threshold voltage at room temperature for V_{SB}=0. Use $_{si} \quad 11.7\;_0$

SOLUTION :

$$_F \; (substrate) \quad \frac{kT}{q}\ln\frac{N_{D,sub}}{n_i} \quad 0.026\ln\frac{1\;10^{16}}{1.45\;10^{10}} \quad 0.348[\text{V}]$$

$$_F \; (gate) \quad \frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} \quad 0.026\ln\frac{1\;10^{20}}{1.45\;10^{10}} \quad 0.587[\text{V}]$$

$$_{GC\,F}(substrate) \; _F(gate) \quad 0.348 \quad 0.587 \quad 0.239[\text{V}] \quad C_{ox} \; _{ox} \quad \frac{3.9}{8.85\;10^{14}} \quad 3.45\;10^{8}\,[F/cm^2]$$

$$t_{ox} \qquad 0.1\;10^{4}$$

$$Q_{B0} \sqrt{2\, qN_{D,sub\ si} |2_{F}|}$$

$$\sqrt{2\ 1.6\ 10^{19}\ 10^{16}\ 11.7\ 8.85\ 10^{14}\ 2\ 0.348} \quad 4.8\ 10^{8}$$

$$[C / cm^2]$$

$$V_{T0} \quad 2_{F} \quad \frac{Q_{B0}}{C_{ox}} \cdot \frac{Q_{ox}}{C_{ox}}$$

$$0.239\ \ 2\ \ 0.348 \quad \frac{4.8\ \ 10^{8}}{3.45\ \ 10^{8}} \cdot \frac{4\ \ 10^{10}\ \ 1.6\ \ 10^{19}}{3.45\ \ 10^{8}}$$

2.51[V]

3.10 Using the parameters given, calculate the current through two nMOS transistors in series (see Fig. P3.11), when the drain of the top transistor is tied to V_{DD}, the source of the bottom transistor is tied to V_{SS} = 0 and their gates are tied to V_{DD}. The substrate is also tied to V_{SS} = 0 V. Assume that W/L = 10 for both transistors and L=4 m.

k' = 168 A/V$_2$
V_{T0} = 0.48 V
= 0.52 V$_{1/2}$
$|2_{F}|$ = 1.01 V

Hint : The solution requires several iterations, and the body effect on threshold voltage has to be taken into account. Start with the KCL equation.

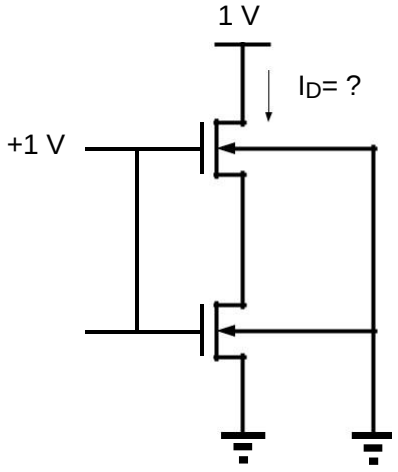


Figure P3.10

SOLUTION :

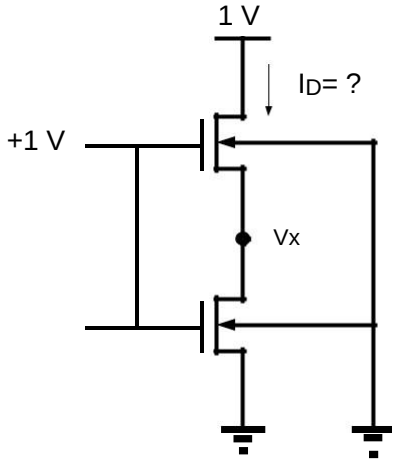


Figure P3.10

Since gate voltage is high, the midpoint V_x is expected to be low. Therefore, the load is in saturation and the driver is in linear region. From KCL

$$I_D I_{D,\,driver} \quad I_{D,\,load}$$

$$\frac{1}{2} k' \frac{W}{L} 1\ V_x \qquad V_{T,L}(V_x)^2 \frac{1}{2} k' \frac{W}{L} \quad 2\,1\ V_{T0}\ V_x\ V_x^2$$

Using the following two equations to iterate find the solution.

$$1\ V_x \quad V_{T,L}(V_x)^2 \quad 1.04V_x \quad V_x{}_2$$

$$V_{T,L}(V_x)\ 0.48\ 0.52 \quad \sqrt{1.01\ V_x} \quad \sqrt{1.01}$$

The intermediate values are listed in the table:

$V_{T,L}(V_x)$	V_x
0.480	0.1523
0.518	0.1337
0.513	0.1359
0.514	0.1357
0.514	0.1357

$$I_D \quad \frac{1}{2} k' \frac{W}{L} (1.04V_x \quad V_x^2)\ 0.5\ 168\ 10\ 1.04\ 0.1357\ 0.1357^2 \quad 103.1[\ A]$$

3.11 The following parameters are given for an nMOS process:

t_{ox} = 16 Å
substrate doping $N_A = 4 \cdot 10^{18}$ cm^{-3}
polysilicon gate doping $N_D = 2 \cdot 10^{20}$ cm^{-3}
oxide-interface fixed-charge density $N_{ox} = 2 \cdot 10^{10}$ cm^{-3}

(a) Calculate V_T for an unimplanted transistor.
(b) What type and what concentration of impurities must be implanted to achieve V_T = + 0.6 V and V_T = – 0.6 V ?

SOLUTION :

(a) For unimplanted transistor,

$$\phi_F(\text{substrate}) = \frac{kT}{q}\ln\frac{N_A}{n_i} = 0.026\text{V}\ln\frac{4\times10^{18}}{1.45\times10^{10}} = 0.51\text{V}$$

$$\phi_F(\text{gate}) = \frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} = 0.026\text{V}\ln\frac{2\times10^{20}}{1.45\times10^{10}} = 0.61\text{V}$$

$$\phi_{GC} = \phi_F(\text{substrate}) + \phi_F(\text{gate}) = 0.51\text{V} + 0.61\text{V} = 1.12\text{V}$$

$$Q_{B0} = -\sqrt{2q\varepsilon_{Si}N_A\left|2\phi_F(\text{substrate})\right|}$$

$$= -\sqrt{2\times1.6\times10^{-19}\times(4\times10^{18})\times11.7\times8.85\times10^{-14}\times\left|2\times0.51\right|} = -1.16\times10^{-6}\ \text{C/cm}^2$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97\times8.85\times10^{-14}\ \text{F/cm}}{1.6\times10^{-7}\ \text{cm}} = 2.2\times10^{-6}\ \text{F/cm}^2$$

$$V_{T0} = \phi_{GC} - 2\phi_F(\text{substrate}) - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$= 1.06 - (-1.12) - (-0.53) - (0.03) = 0.56\text{V}$$

(b) For V_T= 2V;

$$V_T = 2 - V_{T0} - \frac{Q_{II}}{C_{ox}} = 0.56 - \frac{Q_{II}}{C_{ox}}$$

Negative charges needed in this case, so it must be p-type implant in the amount of

$$Q_{II} = qN_I(V_T - V_{T0})C_{ox}$$

$$N_I = (2 - 0.56)\frac{2.2\times10^{-6}}{1.6\times10^{-19}} = 1.98\times10^{13}\ cm^{-3}$$

For V_T=-2V, positive charges need, must be n-type implant,

$$N_I = (-2 - 0.56)\frac{2.2\times10^{-6}}{1.6\times10^{-19}} = 3.52\times10^{13}\ cm^{-3}$$

3.12 Using the measured data given, determine the device parameters V_{T0}, k, , and assuming $_F$ = – 1.1 V and L=4 m.

V_{GS} (V)	V_{DS} (V)	V_{BS} (V)	I_D(A)
0.6	0.8	0	8
0.8	0.8	0	59
0.8	0.8	-0.3	37
0.8	1.0	0	60

SOLUTION :

Because the given device is a long channel device, when $V_{DS} \geq V_{GS}$, the transistor operates in saturation region, therefore

$$I_{DSAT} \quad \frac{k}{2} V_{GS} \quad V_T \ ^2 \ 1 \quad V_{DS}$$

a) Find

$$\frac{I_{DSAT} \ Row\ 4}{I_{DSAT} \ Row\ 2} \quad \frac{1 \quad V_{DS} \ Row4}{1 \quad V_{DS} \ Row2} \quad \frac{1}{1\,0.8} \quad \frac{60}{59}$$

$$1$$

$$0.09 \ V$$

b) Find V

$$\frac{I_{DSAT} \ Row\ 2}{I_{DSAT} \ Row1} \quad \frac{0.8 \ V_{T0} \ ^2}{0.6 \ V_{T\,0} \ _2}$$

V_{T0}=0.48V

c) Find k:
From Row2 data,

$$59 \quad \frac{k}{2} 0.8 \ 0.48^2 1 \ 0.09 \ 0.8$$

$$k \ 1.08 \ \text{mA/V}^2$$

d) Find :
From Row3 data,

$$37 \quad \frac{1075}{2} 0.8 \ V_T \ (V_{BS} \quad 0.3) \ ^2 \ 1 \quad 0.09 \ 0.8$$

$$V_T \ (V_{BS} 0.3) \quad 0.55 \ \text{V}$$

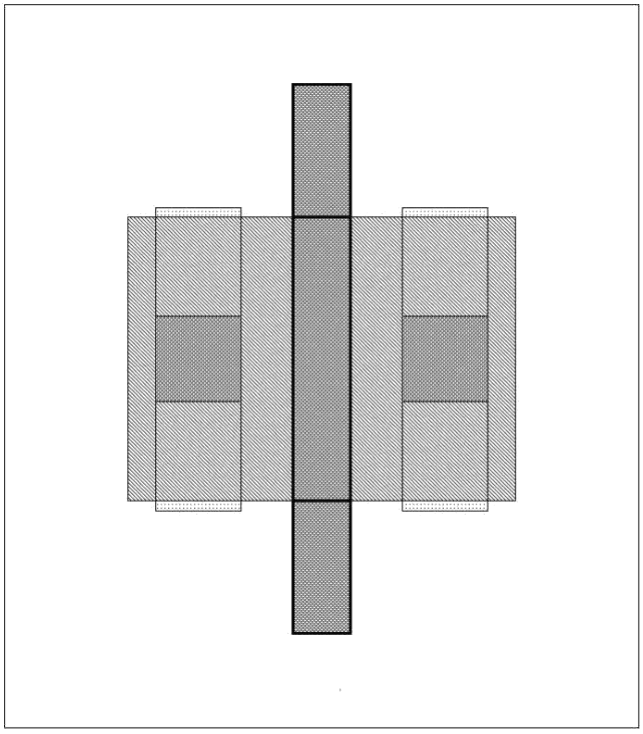
$$0.55 \quad 0.48 \quad \sqrt{0.3 \ 1.1} \ 1.1$$

$$0.52 \ \text{V}^{1/2}$$

3.13 Using the design rules specified in Chapter 2, sketch a simple layout of an nMOS transistor on grid paper. Use a minimum feature size of 60 nm. Neglect the substrate connection. After you complete the layout, calculate approximate values for C_g, C_{sb}, and C_{db}. The following parameters are given.

Substrate doping $N_A = 4 \cdot 10^{18}$ cm^{-3}
Drain/source doping $N_D = 2 \cdot 10^{20}$ cm^{-3}
W = 300 nm
L = 60 nm
t_{ox} = 1.6 nm
Junction depth = 32 nm
Sidewall doping = $4 \cdot 10^{9}$ cm^{-3}
Drain bias = 0 V

SOLUTION :



Because the drain bias is equal to 0V, there is no current in the device.
First of all, C_{ox} is calculated like below:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97\ 8.85\ 10^{-14}\ \text{F/cm}}{1.6\ 10^{-7}\ \text{cm}} = 2.2 \quad 10^{-6}\ \text{F/cm}^2$$

So total gate capacitance Cg is

$$C_g = C_{gb} + C_{gd} + C_{gs}$$

$$C_{ox}WL + C_{ox}WL_D + C_{ox}WL_D$$

$$C_{ox}WL \quad (\text{total length})$$

$$2.2\ 10^{-2}\ \text{F/m}^2\ 300\ 10^{-9}\ \text{m}\ 60\ 10^{-9}\ \text{m}$$

$$0.396\text{fF}$$

$$_0 = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2} = 0.026\text{V}\ \ln\frac{4\ 10^{18}\ 2\ 10^{20}}{2.1\ 10^{20}} = 1.11\text{V}$$

$$_{0sw} = \frac{kT}{q}\ln\frac{N_A(sw)\,N_D}{n_i^2} = 0.026\text{V}\ \ln\frac{4\ 10^{9}\ 2\ 10^{20}}{2.1\ 10^{20}} = 0.57\text{V}$$

$$C_{j0} \sqrt{\frac{Si\ q}{2} \frac{N_A N_D}{N_A N_D} \frac{1}{0}}$$

$$\sqrt{\frac{11.7\ 8.85\ 10^{14}\ \text{F/cm}\ 1.6\ 10^{19}}{2} \frac{4\ 10^{18}\ 2\ 10^{20}}{4\ 10^{18}\ 2\ 10^{20}} \frac{1}{1.11\text{V}}}$$

$54.1\ 10^{8}\ \text{F/cm}^2$

$$C_{j0sw} \sqrt{\frac{Si\ q}{2} \frac{N_A N_D}{N_A N_D} \frac{1}{0}}$$

$$\sqrt{\frac{11.7\ 8.85\ 10^{14}\ \text{F/cm}\ 1.6\ 10^{19}}{2} \frac{4\ 10^{9}\ 2\ 10^{20}}{4\ 10^{9}\ 2\ 10^{20}} \frac{1}{0.57\text{V}}}$$

$24.1\ 10^{12}\ \text{F/cm}^2$

The zero-bias sidewall junction capacitance per unit length can also be found as follows.

$$C_{jsw} \quad C_{j\,0sw}\ x_j \qquad 24.1\ 10^{12}\ \text{F/cm}^2\ \ 32\ \ 10^{7}\ \text{cm} \quad 77.15\text{aF/cm}$$

The total area of the n + /p junctions is calculated as the sum of the bottom area and the sidewall area facing the channel region.

$$A \quad (0.3\ 0.15)\ \text{m}^2\ (0.15\ 0.032)\ \text{m}^2\ 0.05\ \text{m}^2\ P\ 2\ 0.3\ \text{m}\ 0.15\ \text{m}\ 0.75\ \text{m}$$

$$C_{db} \quad A\ C_{j\,0} \quad P\ C_{jsw}$$

$$0.05\ \ 10^{8}\ \text{cm}^2\ \ 54.1\ 10^{8}\ \text{F/cm}^2 \qquad 0.75\ \ 10^{4}\ \text{cm}\ 77.2\ \ 10^{18}\ \text{F/cm} \qquad 0.271\ 10^{15}\ \text{F}$$

$0.271\text{fF}\ \ C_{sb}$

3.14 An enhancement-type nMOS transistor has the following parameters:

V_{T0} = 0.48 V
= 0.52 $V_{1/2}$
= 0.05 V_{-1} |2
$_F|$ = 1.01 V k' =
168 A/V_2

(a) When the transistor is biased with V_G = 0.6 V, V_D = 0.22 V, V_S = 0.2 V, and V_B = 0 V, the drain current is I_D = 24 A. Determine W/L.

(b) Calculate I_D for V_G = 1 V, V_D = 0.8 V, V_S = 0.4 V, and V_B = 0 V.

(c) If n = 76.3 cm^2/V·s and $Cg = C_{OX} \cdot W \cdot L$ = 1.0 x 10^{-15} F, find W and L.

SOLUTION :

(a) For enhancement transistor and $V_{T0} > 0$, it must be nMOS.

$$V_T = V_{T0} + \sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}$$

$$0.48 + 0.52\left(\sqrt{1.01 + 0.2} - \sqrt{1.01}\right) = 0.529 \text{ V}$$

$$V_{DS} \geq V_{GS} - V_T = 0.6 - 0.52 = 0.08$$

nMOS transistor is in saturation.

$$I_{D\,sat} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$\frac{W}{L} = \frac{2I_D(sat)}{k'(V_{GS} - V_T)^2(1 + \lambda V_{DS})}$$

$$\frac{2(24 \times 10^{-6})}{168 \times 10^{-6}(0.08)^2(1 + 0.05 \times 0.8)} = 42.92$$

(b)

$$V_T = V_{T0} + \sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}$$

$$0.48 + 0.52\left(\sqrt{1.01 + 0.4} - \sqrt{1.01}\right) = 0.575 \text{ V}$$

$$V_{DS} \geq V_{GS} - V_T = 0.6 - 0.575 = 0.025$$

nMOS transistor is in linear region.

$$I_D = \frac{k'W}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right](1 + \lambda V_{DS})$$

$$\frac{84 \times 10^{-6}}{2}(42.92)\left[2(0.025)(0.02) - (0.02)^2\right](1 + 0.05 \times 0.02)$$

$$= 2.16\ \mu A$$

(c)

$$C_{ox} = k' = \frac{168 \times 10^{-6}}{\sqrt{76.3}} = 2.2 \times 10^{-6} \text{ F/cm}^2$$

$$\frac{W}{L} = \frac{C_g}{C_{ox}} = \frac{10^{-15}}{2.2 \times 10^{-6}} = 4.5 \times 10^{-8} \text{ F/cm}^2$$

$$\frac{W}{L} = 42.92$$

Solve for W and L,

$$W = 14.2\ \mu m$$

$$L = 0.33\ \mu m$$

3.15 An nMOS transistor is fabricated with the following physical parameters:

$$N_D = 2.4 \cdot 10^{18}\ \text{cm}^{-3}$$

N_A(substrate) = $2.4 \cdot 10^{18}$ cm^{-3}

N^+_A(chan. stop) = 10^{19} cm^{-3}

W =400 nm

Y = 175 nm

L = 60 nm

L_D = 0.01 m

X_j = 32 nm

(a) Determine the drain diffusion capacitance for V_{DB} = 1.2 V and 0.6 V.

(b) Calculate the overlap capacitance between gate and drain for an oxide thickness of t_{OX} = 18 Å.

SOLUTION :

(a)

$$0 \frac{kT}{q} \ln \frac{N_A N}{n_i 2} \cdot \frac{n}{2.1\ 10^{20}} 0.026V \ln \frac{2.4\ 10^{18}\ 2.4\ 10^{18}}{2.1\ 10^{20}} 984\ mV$$

$$C_{j0} \sqrt{\frac{Si\ q}{2} \frac{N_A\ N_D}{N N} \frac{1}{0}}$$

$$\sqrt{\frac{11.7\ 8.85\ 10^{14}\ F/cm\ 1.6\ 10^{19}}{2} \frac{2.4\ 10^{18}\ 2.4\ 10^{18}}{2.4\ 10^{18}\ 2.4\ 10^{18}} \frac{1}{984mV}}$$

$$31.8\ 10^{8}\ F/cm^{2}$$

$$A\ W Y\ W\ X_j \quad 0.4\ 0.175\ 0.4\ 0.32 \quad 0.198\ m^2$$

$$C_j\ V \frac{A C_{j0}}{\sqrt{1\ \frac{V}{0}}}$$

$$C_j\ 1.2 \frac{0.198\ 10^{8}\ 31.8\ 10^{8}}{\sqrt{1\ \frac{1.2}{0.984}}} \quad 0.423\ 10^{15}\ F$$

$$C_j\ 0.6 \frac{0.198\ 10^{8}\ 31.8\ 10^{8}}{\sqrt{1\ \frac{0.6}{0.984}}} \quad 0.496\ 10^{15}\ F$$

For sidewall capacitance calculation,

$$_{osw} \frac{kT}{q} \ln \frac{N_A\ sw\ N_D}{n_i 2} \quad 0.026V \ln \frac{10^{19}\ 2.4\ 10^{18}}{2.1\ 10^{20}} \quad 1.02\ V$$

$$C_{josw}$$

$$\sqrt{\frac{Si \; q \quad N_A \; sw \; N_D \quad 1}{2 \quad N_A \; sw \; N_D \quad osw}}$$

$$\sqrt{\frac{11.7\ 8.85\ 10^{-14}\ F/cm\ \ 1.6\ 10^{-19} \quad 2.4\ 10^{18}\ 10^{19} \quad 1}{2 \qquad\qquad 2.4\ 10^{18} \quad 10^{19} \quad 1.02V}}$$

$$39.6\ 10^{-8}\ F/cm^{2}$$

$$C_{jsw}(V) \quad \frac{P\ X_j \quad josw}{\sqrt{1-\frac{V}{osw}}} \quad \frac{2\ 175\ 400\ 10^{-7}\ 32\ 10^{-7}\ 39.6\ 10^{-8}}{\sqrt{1-\frac{V}{osw}}}$$

$$\frac{1.77\ 10^{-14}\ V}{\sqrt{1-\frac{}{osw}}}\ F$$

$$C_{jsw}(1.2V) \quad \frac{1.77\ 10^{-14}}{\sqrt{1-\frac{1.2}{1.02}}} \quad 12\ 10^{-15}\ F$$

$$C_{jsw}(0.6V) \quad \frac{1.77\ 10^{-14}}{\sqrt{1-\frac{0.6}{1.02}}} \quad 14\ 10^{-15}\ F$$

$$\langle C \rangle \quad 1.2V \quad C_j \quad 1.2V \quad C_{jsw} \quad 1.2V \quad 0.423 \quad 12 \quad 12.423\ fF$$

$$C_{db} \quad 0.6V \quad C_j \quad 0.6V \quad C_{jsw} \quad 0.6V \quad 0.496 \quad 39.6 \quad 40.096\ fF$$

(b)

$$C_{ox} \quad \frac{ox}{t_{ox}} \quad \frac{3.9\ 8.85\ 10^{-14}}{18\ 10^{-8}} \quad 1.92\ 10^{-6}\ F/cm^3$$

$$C_{gd} \quad C_{ox}\ W\ L_D \quad 1.92\ 10^{-6} \quad 400\ 10^{-7}\ 0.01\ 10^{-4}\ 0.077\ fF$$